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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/010,162

11/20/2001

Fwu-luan Hshieh

GS 149

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27774

7590

01/28/2005

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EXAMINER

ROMAN, ANGEL

ART UNIT

PAPER NUMBER

2812

DATE MAILED: 01/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. <u>10/010,162</u>	Applicant(s) HSHIEH ET AL.	
	Examiner Angel Roman	Art Unit 2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 November 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 12-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 12-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 November 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

1. The drawings were received on 11/21/04. These drawings are acceptable.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 12-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nam et al. U.S. Patent 6,211,018 B1 in view of Silicon Processing for the VLSI Era, Optical Photoresist Material Types, Pages 418-420, hereinafter vlsi.

Regarding claims 12 and 22, Nam et al. discloses a method of forming a trench MOSFET comprising; providing a silicon semiconductor wafer 71 of a first conductivity type N^+ ; depositing a silicon epitaxial layer 72 of said first conductivity type over said wafer 71, said epitaxial layer 72 having a lower majority carrier concentration N^- than said wafer 71; forming a body region 75 of a second conductivity type P within an upper portion of said epitaxial layer 72; providing a patterned first silicon oxide (densified non-doped silica glass) masking material layer 73 over said epitaxial layer 72, said patterned first masking material layer 73 comprising a first aperture (see figure 5A) and being overlaid by a photoresist material (see column 6, lines 10-12); depositing a second silicon oxide (densified non-doped silica glass) masking material layer 77 over said first masking material layer 73; plasma ion etching said second masking material layer until an aperture is created in said second masking material layer within said first aperture (see figure 5C); forming a trench in said epitaxial layer by etching through said second aperture; forming an insulating layer 78 lining at least a portion of said trench; forming a conductive region 79 within said trench adjacent said insulating layer 78; and forming a source region 81 of said first conductivity type N within an upper portion of said body region 75 and adjacent said trench, wherein said source region is formed after forming

the trench and wherein a lateral thickness of said source region 81 is independent of the measurement of the distance between the first and second apertures (see figure 5E).

Regarding claim 13, Nam et al. discloses providing said patterned first masking material over the semiconductor wafer by providing a first masking material layer 73 over said epitaxial layer 72; applying a patterned photoresist layer over said first masking material layer 73; and etching said first masking material layer 73 through an aperture in said patterned photoresist layer such that said first aperture is formed in said first masking material layer 73 (see column 6, lines 6-16).

Regarding claim 14, Nam et al. discloses said semiconductor wafer being a silicon wafer (see column 6, line 9) and the epitaxial layer 72 being a silicon epitaxial layer (see column 6, line 7).

Regarding claims 15, 16 Nam et al. discloses the first and second masking materials being of the same material composition (silicon dioxide).

Regarding claims 17, 18 and 20, Nam et al. discloses using an anisotropic dry oxide etching process to etch the first and second masking materials and the semiconductor (see column 6, lines 14-16, 32-34 and 42-43).

Regarding claims 12, 22 and 19, Nam et al. is applied as above but lacks anticipation on disclosing a positive photoresist material being used as the photoresist. VLSI discloses positive photoresist materials as a dominant photoresist for VLSI applications, therefore, it would have been obvious to a person having ordinary skills in the art at the time the invention was made to disclose a positive photoresist material as the photoresist used in the primary reference of Nam et al. since it would prevent

contamination of unexposed regions (see vlsi page 419). Furthermore selecting a particular type of material used for the photoresist, is only considered to be the use of a " preferred " or " optimum " material out of a plurality of well known materials that a person having ordinary skill in the art at the time the invention was made would have find obvious to provide using routine experimentation.

Regarding claim 21, Nam et al. is applied as above and discloses first and second trench mask apertures having a width but does not disclose a particular value for this parameter. However, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to provide a width ranging from 0.4-0.8 microns in smallest dimension for the first trench mask aperture and the second trench mask aperture having a width ranging from 0.2-0.6 microns, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the "optimum range" involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Response to Arguments

6. Applicant's arguments with respect to claims 12-22 have been considered but are moot in view of the new ground(s) of rejection.

7. Applicant's argue that Nam et al. does not disclose first and second masking layers comprising densified non-doped silica glass, however Nam et al. clearly teaches using silicon dioxide as the material for the first and second masking layers and silicon dioxide is commonly known as undoped silica glass (see Iyer U.S. 5,629,246A, column

1, lines 14-16) and annealing processes following the masking layer deposition which densified the deposited silicon dioxide masking layers.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Iyer discloses a relationship between silica and silicon dioxide.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel Roman whose telephone number is (571) 272-1681. The examiner can normally be reached on Monday-Friday 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AR
January 24, 2005


MICHAEL S. LEBENTRITT
PRIMARY EXAMINER
SP 2812